

## THE INDUCTIVE CONNECTION EFFECTS OF A MOUNTED SPDT IN A PLASTIC SO8 PACKAGE

F. NDAGIJIMANA, J. ENGDAHL, A. AHMADOUCHE, J. CHILO

LEMO - ENSERG, B.P. 257, 38016 Grenoble Cedex - FRANCE  
Phone (33) 76 85 60 27, Fax (33) 76 85 60 80

### ABSTRACT

An investigation of the electrical performances of an assembled SO8 package is presented. Using an equivalent electric network elaborated for the whole assembly, the isolation and the insertion losses are computed for a signal frequency up to 5 GHz. From our modelling and simulation results, the significant effect of the path connection to ground is shown, and the required modifications of the connecting layout are discussed. Our modelling concept, demonstrated on the SO8 package, is applicable on any single chip package.

### INTRODUCTION

The electrical modelling of interconnections for integrated circuits on printed board is essential before costly hardware is committed. Using modelling techniques such as Method of Moments [1-2], electrical parameters of each part of the package are extracted [3-4], and an equivalent network of the whole assembly can be elaborated. Then it is possible to predict the frequency limitations of the assembly and to propose the required modifications of the connecting layout. This modelling technique has been applied on a high speed assembly including SO8 package and SPDT integrated switch [5]. In reference 5, the insertion losses and the isolation have been calculated for a

signal frequency up to 5 GHz. The analysis of the modelling results permitted to point out the importance of the path connection to ground, which is responsible of the weak isolation. This paper is focussed on that inductive connection effects on the electrical performances of single chip assemblies, demonstrated on the SO8 package.

### THE ANALYSED STRUCTURE :

The analysed structure is based on the plastic SO8 package used for CMS applications assembled with a Single Pole-Double Throw (SPDT) switch integrated circuit (fig.1).

A typical transversal cross-section of the structure is given in figure 2 a-b; it shows the position of the IC with respect to the main ground.

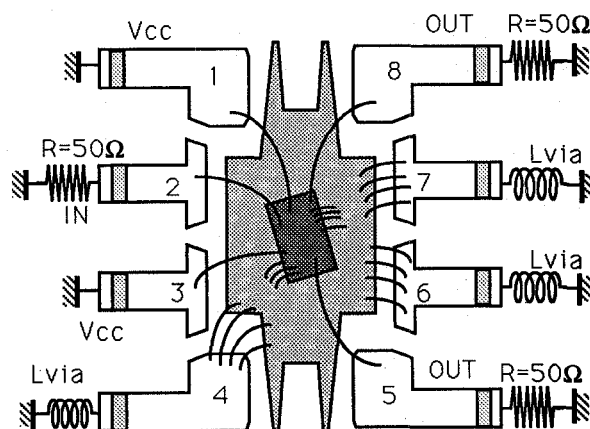


Fig. 1 The assembled SO8 package (top view)

Figure 2-a :  
Dimensions in the transversal  
cross-section of the lead frame

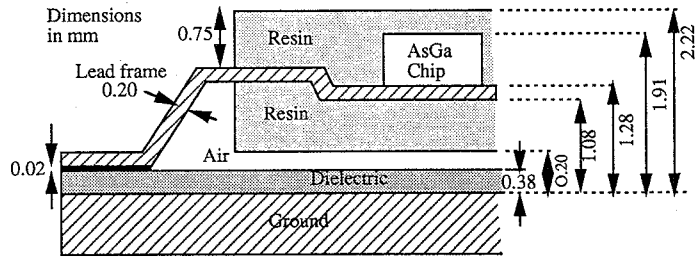
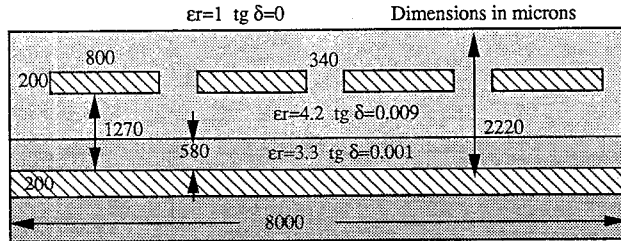


Figure 2-b :  
Transversal cross-section of  
the lead frame



The equivalent network of the SPDT switch (1 input, 2 outputs) is represented in figure 3. The electrical parameters  $R_{on}=12 \Omega$ ,  $C_{off}=136 \text{ fF}$  are determined experimentally, by direct on wafer measurements : 1.2 dB of insertion losses, 35 dB of isolation at 2 GHz.

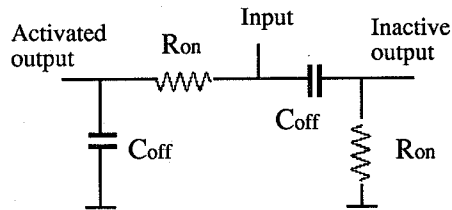


Figure 3 : Equivalent network of the SPDT switch

In reference [5], an equivalent lumped network of the whole package (consisting of inductances and capacitances) has been elaborated. For each part of the lead frame the L and C are calculated from the geometrical and the technological parameters. A summary of the typical values is given below:

- inductance of a single lead  $L_t=0.7 \text{ nH}$
- capacitance of a single lead  $C_t=45 \text{ fF}$
- Inductance of a wire bonding  $L_B=1.1 \text{ nH}$
- inductance of a via hole  $L_v=51 \text{ pH}$

If we neglect the coupling effect between strips a simplified equivalent circuit can be given for the strip and the wire bonding (figure 4).

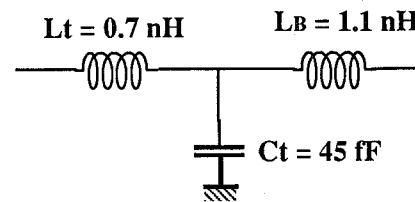


Figure 4 : Simplified equivalent network for a strip in the lead frame

## STUDY OF THE WHOLE ASSEMBLY

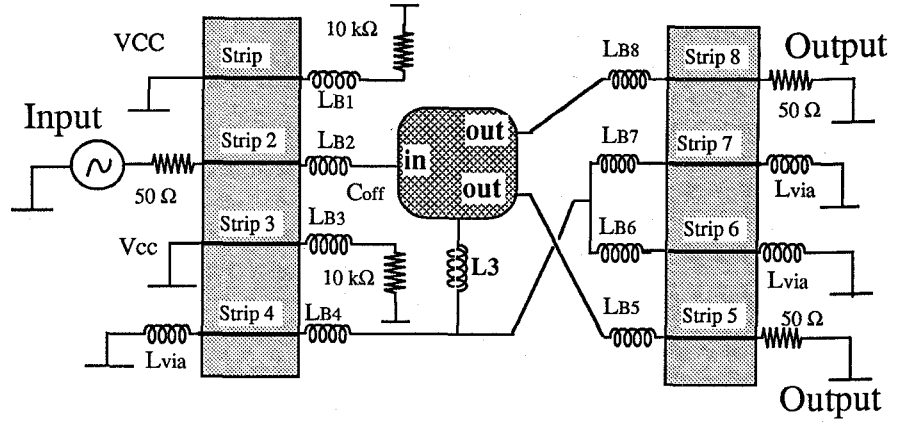
We supposed that the signal is applied on pin 2 and pin 8 is the path "ON" and pin 5 is the path "OFF"(Fig. 1). The equivalent network of the assembly is presented in figure 5. The DC supply is supposed to be ideal and the power consumption is simulated with 10 K $\Omega$  resistances.

### Influence of the inductive ground connection;

The mounted SPDT is connected to ground via the die (the fictitious ground plane) and through the lead frame as shown in figure 5.

The influence the path connection to ground can be easily deduced from the two simple circuits presented in figure 6 : for an ideal transformer, the voltages V1 and V2 are given by the relation :

Figure 5 : Equivalent circuit for the whole assembly



$$V1 = j\omega L1 i1 + j\omega M i2$$

$$V2 = j\omega M i1 + j\omega L2 i2$$

where  $M$  is the mutual coupling between  $L1$  and  $L2$ .

If  $L1 = L2 = L$  the coupling factor is  $K = M/L$

For non coupled inductances with common inductance  $L_G$ , the voltages  $V1$  and  $V2$  are given by:

$$V1 = j\omega (L1 + L_G) i1 + j\omega L_G i2$$

$$V2 = j\omega L_G i1 + j\omega (L2 + L_G) i2$$

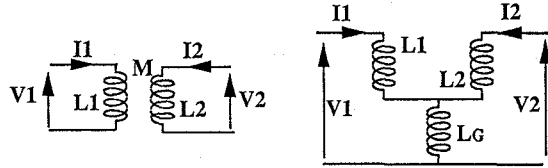


Figure 6 : Analogy between an ideal transformer and a circuit with a common inductance

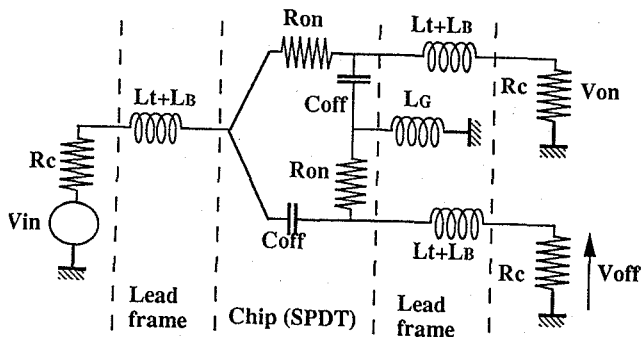


Figure 7 : Simplified equivalent network for the insertion losses and the isolation analysis.

If  $L1 = L2 = L_G = L$ , the coupling factor due to the presence of  $L_G$  is  $K_B = L_G / (L + L_G)$ .

For the assembled So8 package, the common inductance is consists of three parallel wire bondings connected to pin 4, 6 and 7. If the inductance  $L3$  is negligible compared to  $L_t + L_B$ , we have an equivalent inductance  $L_G \approx L/3$ . Then the associated coupling factor is  $K_B = 25\%$  (in our case  $L = L_t + L_B$ ).

Figure 7 shows a simplified equivalent circuit which can be used for the insertion losses and the isolation analysis.

### Insertion losses:

The insertion losses are extracted using the equivalent network of the whole assembly, as a function of the frequency, and for different values of the common inductance  $L_G$ . At 2 GHz the global device has 1.4 dB losses, the switch has 1.2 dB losses (fig.2), and the SO8 package introduces only 0.2 dB additional losses. This performance seems acceptable for our application.

From the results shown in figure 8, we conclude that the insertion losses are little sensitive to the common inductance  $L_G$  up to 3.0 GHz. For higher frequencies, the effect of this inductance becomes important.

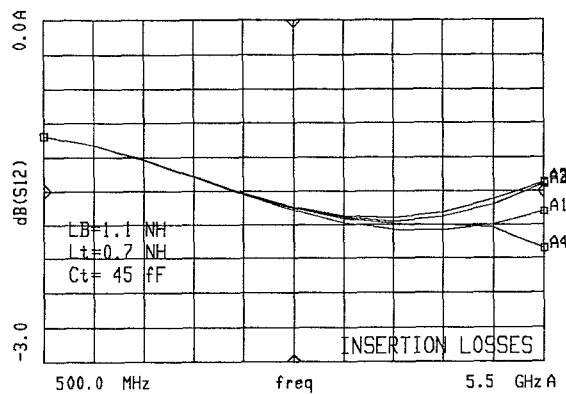


Figure 8 : The insertion losses for different values of the common inductance  $L_G$

### **Isolation :**

The isolation is defined as the transmission along the path "OFF", and the results are given in figure 9; the isolation is as expected very dependent on the common inductance  $L_G$ .

We can notice that at 2 GHz the device has about 22 dB of isolation for  $L_G=2$  nH. The switch having 35 dB of isolation, hence, the S08 package isolation reduction is 13 dB. This reduction of isolation is mainly due to the value of  $L_G$  : for  $L_G=0$  (ideal case), the isolation is about 31 dB. The effect of the wire bondings corresponds to an isolation reduction of about 4 dB.

### **CONCLUSION**

The agreement obtained between the experimental results and the simulations show how accurate our modelling concept is. On the investigated assembly, the results show that the S08 package is suitable for applications up to 2 GHz (1.4 dB of insertion losses and 22 dB of isolation).

The analysis of the insertion losses shows that the inductive bondings are the main sources of this limitations. It is a must to reduce these inductive bonding effects when higher frequencies are planned (reduction of the length and the distance to the ground).

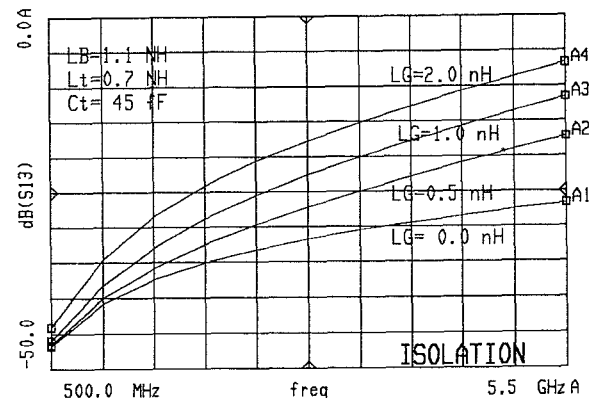


Figure 9 : The isolation for different values of the common inductance  $L_G$

The simulation reveals the significant effect of the inductances connecting the chip to the die, and the die to the principal ground plane through the lead frame. The best way to improve the electrical performances of the mounted IC is therefore to reduce these inductances, may be by direct connecting the ground die to the main (global) ground plane.

### **REFERENCES**

- [1] T. ITOH  
Numerical Techniques for Microwave and Millimeter-Wave Passive structure  
J Wiley and Son
- [2] R.F HARRINGTON  
Field Computation by Moment Method  
Collier-Mc Millan New York 1968
- [3] J. CHILO and T. ARNAUD  
Coupling effects in time domain of an interconnecting bus in high speed GaAs logic Circuits  
IEEE Trans electron Devices, Vol ED-31, March 1984
- [4] A. AHMADOUCHE, J. CHILO  
Optimum computation of capacitance coefficients of multilevel interconnecting lines for advanced packages  
IEEE, CHMT-12 No 1, March 1989
- [5] F. NDAGIJIMANA, J. ENGDAHL, A. AHMADOUCHE, J. CHILO  
Frequency limitation on an assembled SO8 package  
Proceeding of ECTC, Orlando, June 1993